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Docket FR9200200061US1

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	R. Gallezot et al.	Art Unit No.:	2133
Application No.:	09/548,908	Examiner:	J.D. Torres
File Date:	27 February 2002	Customer No.	25299

For: System and Methods for Enabling Computation of CRC's N-bit at a time

Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

AMENDMENT TRANSMITTAL & PETITION FOR EXTENSION OF TIME

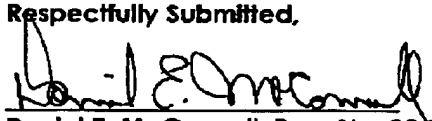
Transmitted herewith is an amendment for this application.

1. The fee for claims has been calculated as shown below:

Claims Remaining After Amendment (27+3 for multi-dependencies)		Highest Number Already Paid For (27+3 for multi-dependencies)	Present extra	Rate	Additional Fee
Total	16	20	0	$50.00	$0.00
Indep	2	3	0	$200.00	$0.00
First Presentation of Multiple Dependent Claims? No				$360.00	$0.00
TOTAL:					$0.00

Please charge Deposit Account Number 50-0563 for the fees as set forth above. The Commissioner is authorized to charge payment of any additional fees required under 37 CFR §1.16 and 37 CFR §1.17 or to credit any overpayment to the designated Deposit Account. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,



Daniel E. McConnell, Reg. No. 20,360
Telephone (919) 510-4246

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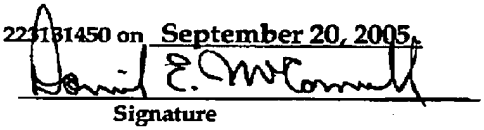

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By Daniel E. McConnell

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	Date: September 20, 2005
R. Gallezot et al	:	Group Art Unit: 2133
Serial Number: 10/084,543	:	Examiner: J.D. Torres
Filed: 27 February 2002	:	INTERNATIONAL BUSINESS MACHINES CORPORATION
Title: System and Methods for Enabling Computation of CRC's –bit at a Time	:	Intellectual Property Law Department D-YXSA B-002/2 P.O. Box 12195
	:	Research Triangle Park, NC 27709

Amendment After Final

The Commissioner of Patents
Box AF
P.O. Box 1450
Alexandria, VA 2213-1450

Dear Sir:

Responsive to the Notification of Non-Responsive appeal Brief mailed September 7, please enter an amendment as follows:

Amendments to the Claims:

1 (Previously presented). A method of performing a Cyclic Redundancy Check (CRC) calculation, said CRC calculation done with N-bit at a time [500] over a binary string of data bits [520], said CRC calculation based on a generator polynomial G(X) [130] of degree d [131], said CRC calculation having intermediate and final results fitting a d-bit wide Field Check Sequence (FCS) [120], said generator polynomial allowing to form a multiplicative cyclic group comprised of d-bit wide binary vectors [400], said method comprising the steps of:

picking [1100] a new N-bit chunk of data bits from said binary string of data bits;

dividing [1110], modulo said generator polynomial G(X), said new N-bit chunk of data bits thus, getting a d-bit wide division result [535];

generating a value for FCS displaced within said cyclic group of d-bit wide binary vectors;

adding [1130], modulo two, said d-bit wide division result and said displaced d-bit wide FCS so generated;

updating [1140] said d-bit wide FCS;

checking if more data bits of said binary string of data bits are left for calculation:

if yes [1151], repeating all recited steps;

if not [1152], exiting the method after checking step;

thereby, getting a final result of said CRC calculation in said d-bit wide FCS.

2 (Previously presented). The method according to claim 1 wherein said final result is utilized to generate said d-bit wide FCS [510] for said binary string of data bits.

3 (Previously presented). The method according to claims 1 or 2 wherein said final result is a checking result of said binary string of data bits [520] including said d-bit wide FCS [510].

4 (Previously presented). The method according to claim 1 wherein said dividing step is omitted, if value of said N-bit is equal to said degree d.

5 (Previously presented). The method according to claim 4 wherein, if value of said N-bit is lower than said degree d, the further step of: padding said N-bit chunk of data with enough leading zeros to match said d-bit wide FCS [540].

6 (Previously presented). The method according to claim 1 wherein said CRC calculation is done from a most significant bit (MSB) [530] of said binary string of data bits and wherein said generating step includes a forward multiplication [560] of said d-bit wide FCS.